REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-5 and 16-29 are presently active in this case, Claims 1-5 having been amended and Claims 16-29 having been added by way of the present Amendment. Care has been taken such that no new matter has been entered. (See, e.g. page 11 and the figures.)

In the outstanding Official Action, the specification was objected to for the use of the term "stress migration." The Applicant submits that one of ordinary skill in the art is familiar with such a term, as is evidenced by the article entitled, "Stress Migration and the Mechanical Properties of Copper" (presented at the 2005 IEEE INTERNATIONAL RELIABILITY PHYSICS SYMPOSIUM on April 19, 2005), which is attached hereto for review by the Examiner. As noted in the Introduction of the article, "[h]igh temperature processing of copper dual damascene structures leaves the copper with a large tensile stress due to a mismatch in coefficient of thermal expansion of the materials involved." The article goes on to note that "the stress can relax with time through the diffusion of vacancies leading to the formation of voids," and this phenomenon is commonly referred to as "stress migration." Such voids caused by stress migration can ultimately lead to open circuit failures. Thus, the Applicant submits that this term is not improper, and therefore the Applicant requests the withdrawal of the objection to the specification.

Claims 4 and 5 were objected to for antecedent basis issues. These claims have been amended as suggested on page 3 of the Official Action. The Applicant therefore requests the withdrawal of the objection to Claims 4 and 5.

Claims 1-3 were rejected under 35 U.S.C. 103(a) as being unpatentable over Ueno et al. (U.S. Pub. No. 2003/0008075) in view of Yamato et al. (U.S. Patent No. 6,388,201). Claims 4 and 5 were rejected under 35 U.S.C. 103(a) as being unpatentable over Kato (U.S. Pub. No. 2002/0030978) in view of Ueno et al. For the reasons discussed below, the Applicant requests the withdrawal of the obviousness rejections.

At the outset, the Applicant notes that the Ueno et al. reference was incorrectly listed in the Official Action and the PTO Form 892 as U.S. Pub. No. 2003/0008975. The Applicant's representative contact the Examiner to determine the correct publication number of the Ueno et al. reference, and the Examiner indicated that U.S. Pub. No. 2003/0008075 is the correct number of the reference being cited. Accordingly, the Applicant respectfully requests that the record be corrected to indicate in any future Official Action(s) and in the PTO Form 892 that the Ueno et al. reference having U.S. Pub. No. 2003/0008975 has been made of record in the present application.

Regarding the merits of the obviousness rejections, the basic requirements for establishing a *prima facie* case of obviousness as set forth in MPEP 2143 include (1) there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings, (2) there must be a reasonable expectation of success, and (3)

the reference (or references when combined) must teach or suggest all of the claim limitations. The Applicant submits that a *prima facie* case of obviousness cannot be established in the present case because the references, either when taken singularly or in combination, do not teach or suggest all of the claim limitations, and there is no suggestion or motivation to modify or combine the references in the manner suggested to arrive at the present invention.

Claim 1 advantageously recites a wiring comprising a first metal diffusion-preventing layer formed on an insulating substrate, a metal seed layer formed on the first metal diffusion-preventing layer, a metal wiring layer formed on the metal seed layer, and a second metal diffusion-preventing layer covering the exposed surface including the side surface of the multilayered structure having the metal seed layer and the metal wiring layer, wherein the metal seed layer and the metal wiring layer are surrounded by the first metal diffusion-preventing layer and the second metal diffusion-preventing layer. Claim 2 advantageously recites a wiring comprising the features of Claim 1 where the second metal diffusion-preventing layer not only covers the exposed surface including the side surface of the multilayered structure having the metal seed layer and the metal wiring layer, but also the first metal diffusion-preventing layer. Claim 3 advantageously recites a wiring comprising a first metal diffusion-preventing layer formed on an insulating substrate, a metal wiring layer formed on the first metal diffusion-preventing layer, and a second metal diffusion-preventing layer covering the exposed surface including the side surfaces of the metal wiring layer and the first metal diffusion-preventing layer, wherein the metal wiring layer is surrounded by the

first metal diffusion-preventing layer and the second metal diffusion-preventing layer.

Regarding Claims 1 and 2, the Official Action notes that the Ueno et al. reference does not teach a metal seed layer. Thus, the Official Action notes that the Ueno et al. reference does not teach a metal seed layer formed on a first metal diffusion-preventing layer, a metal wiring layer formed on the metal seed layer, or a second metal diffusion-preventing layer covering the exposed surface including the side surface of the multilayered structure having the metal seed layer, wherein the metal seed layer and the metal wiring layer are surrounded by the first metal diffusion-preventing layer and the second metal diffusion-preventing layer. Furthermore, the Yamato et al. reference does not supplement this deficiency because this reference does not mention or suggest such a seed layer.

Despite noting that the Ueno et al. reference does not teach a metal seed layer as recited in Claims 1 and 2, the Official Action surmises that it would have been obvious to incorporated such a metal seed layer into the structure of the Ueno et al. invention based upon a discussion in the Background of the Invention section of the Ueno et al. reference. However, this conclusion is flawed since it directly contradicts the express teachings in the Ueno et al. reference. Whether or not a metal seed layer is conventionally known or not is not the issue, and is not dispositive of the issue of whether the present invention is obvious. Regardless of whether a prior art seed layer is discussed in the Background of the Invention section of a reference or whether it is discussed in a secondary reference that is being combined with reference, there still must be a motivation to combine these teachings in order to establish *prima facie* obviousness. In the present instance, the Ueno et al. reference is

explicitly teaching away from the use of such a seed layer, as being complicated and costly, and instead teaches a different configuration that completely eliminates the need for such a seed layer. (See, e.g. paragraphs [0027]-[0034].) Thus, one of ordinary skill in the art would not have been motivated to include such a feature in the inventions depicted in Figures 3 and 4, since such a feature would be contrary to the goals of the invention taught in the Ueno et al. reference. Furthermore, the Official Action suggests that one of ordinary skill in the art would have been motivated to include such a seed layer "to improve adhesion;" however, this rationale is clearly incorrect since the Ueno et al. reference in fact already discloses an adhesion layer (27) that performs this function. Thus, one of ordinary skill in the art would not have been motivated to replace the adhesion layer (27) with a seed layer or add a seed layer in addition to the adhesion layer (27), since this would have been directly contrary to the teachings and goals of the Ueno et al. reference a structure that is less costly and less complicated than the structure depicted in Figure 1.

Thus, for at least this reason, the Applicant respectfully submits that a *prima facie* case of obviousness has not been established with respect to Claims 1 and 2.

Furthermore, Claims 1-3 each recite a second metal diffusion-preventing layer covering the exposed surface including the side surfaces of the metal wiring layer, etc. The Official Action notes that the Ueno et al. reference fails to disclose such a feature, and cites the Yamato et al. reference to supplement this deficiency. The Official Action indicates that it would have been obvious to modify the structure of the Ueno et al. reference depicted in Figure 4 thereof to include such a second metal diffusion-preventing layer covering the

exposed surface including the side surfaces of the metal wiring layer "to prevent the conductive layer from being bared." (Presumably citing to column 10, lines 14-16, of the Yamato et al. reference.) However, the Applicant submits that such a motivation does not make sense in the context of the teachings of the Ueno et al. reference in which a first diffusion prevention layer (15) is already present on the side of wiring layer (11) and thus would already serve this function. Accordingly, it is unclear why one of ordinary skill in the art would have been motivated to include an additional feature to serve a function that was already served by an existing feature, absent hindsight considerations based on the teachings of the present invention. As noted in MPEP 2143.01, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestions, or motivation to do so. The prior art must suggest the desirability of the claimed invention. (MPEP 2143.01 I.) The fact that the references can be combined or modified is not sufficient to establish *prima facie* obviousness, unless the prior art suggests the desirability of the combination. (MPEP 2143.01 III.) Recognizing, after the fact, that a modification of the prior art would provide an improvement or advantage, without suggestion thereof by the prior art, rather than dictating a conclusion of obviousness, is an indication of improper application of hindsight considerations. Simplicity and hindsight are not proper criteria for resolving obviousness.

Thus, for at least this reason, the Applicant respectfully submits that a *prima facie* case of obviousness has not been established with respect to Claims 1-3.

Claim 4 of the present application advantageously recites a display device having at least one wiring, comprising electrodes of driving elements arranged to form a matrix, scanning lines connect to the driving elements, and data lines, at least one of which is arranged so that it is surrounded by a first metal diffusion-preventing layer and a second metal diffusion-preventing layer.

The Official Action acknowledges that the Kato reference does not disclose electrodes of driving elements being surrounded by a first metal diffusion-preventing layer and a second metal diffusion-preventing layer. The Official Action supplements this deficiency with the Ueno et al. reference and states that "it would have been obvious to one of ordinary skill in the art, at the time the invention was made, for Kato to include in his invention that electrodes of driving elements being surrounded by a first metal diffusion-preventing layer and a second metal diffusion-preventing layer to prevent degradation of the electrodes." (Page 7 of the Official Action.) However, the Applicant submits that the electrodes of the Kato reference would not suffer from such a problem (and never even mentions such a problem), since the structure thereof is completely different from that of the Ueno et al. reference.

The Kato reference describes a wiring board in which a conductor pattern of a ground potential that extends in a substantially radial form is connected to a plurality of wiring lines, one end of which is connected to a terminal of an integrated circuit, and in which an anisotropic conductive film is formed in a mounting region. The Kato reference describes that the wiring board is mounted in a display device or an electronic device. The wiring board of the Kato reference is structured so that it is joined to a display panel, i.e., the wiring

boards are manufactured individually as separate parts and then joined. The wiring of the Ueno et al. reference is arranged within an interlayer as a unit, and thus requires the diffusion prevention layer and capping layer. However, the features of the Kato reference cited for the teaching of the electrodes of driving elements, scanning lines, and data lines of Claim 4, do not need the diffusion prevention layer and capping layer of the Ueno et al. reference and therefore there is no motivation to combine these teachings absent hindsight considerations.

As noted in MPEP 2143.01, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestions, or motivation to do so. The prior art must suggest the desirability of the claimed invention. (MPEP 2143.01 I.) The fact that the references can be combined or modified is not sufficient to establish *prima facie* obviousness, unless the prior art suggests the desirability of the combination. (MPEP 2143.01 III.) Recognizing, after the fact, that a modification of the prior art would provide an improvement or advantage, without suggestion thereof by the prior art, rather than dictating a conclusion of obviousness, is an indication of improper application of hindsight considerations. Simplicity and hindsight are not proper criteria for resolving obviousness.

Thus, for at least this reason, the Applicant respectfully submits that a *prima facie* case of obviousness has not been established with respect to Claim 4.

The dependent claims are considered allowable for the reasons advanced for the independent claim from which they respectively depend. These claims are further considered allowable as they recite other features of the invention that are neither disclosed nor

suggested by the applied references when those features are considered within the context of their respective independent claim.

Consequently, in view of the above discussion, it is respectfully submitted that the present application is in condition for formal allowance and an early and favorable reconsideration of this application is therefore requested.

Respectfully Submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Gregory J. Maier
Registration No. 25,599
Attorney of Record

Christopher D. Ward
Registration No. 41,367

Customer Number
22850
Tel. (703) 413-3000
Fax. (703) 413-2220
(OSMMN 10/01)

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ATTACHMENT

Stress Migration and the Mechanical Properties of Copper

G. B. Alers[1], J. Sukamto[1], P. Woytowitz[1], X. Lu[2], S. Kailasam[1], J. Reid[1].
[1]Novellus Systems, San Jose, CA., [2]University of Texas, Austin, TX
glenn.alers@novellus.com

ABSTRACT

Variations in the mechanical properties of copper related to plating chemistry and copper thickness are found to control stress migration performance in dual damascene copper interconnects. These observations cannot be explained by vacancy diffusion alone. Instead, the high tensile stress of the copper and elastic vs. plastic energy dissipation needs to be considered to account for the degradation in stress migration.

INTRODUCTION

High temperature processing of copper dual damascene structures leaves the copper with a large tensile stress due to a mismatch in coefficient of thermal expansion of the materials involved. The stress can relax with time through the diffusion of vacancies leading to the formation of voids and ultimately open circuit failures. [1, 2, 3] Controlling this phenomenon requires optimization of several processes including copper annealing, [4] metal barrier deposition process, [5] and interconnect geometry. [6,7] In this paper, it is shown that variations in the plating chemistry and the underlying metal thickness can modulate the stress behavior of copper, which has an impact on via stress migration. Copper with a low yield stress is found to give superior stress migration performance due to the plastic dissipation of local stress in the copper.

EXPERIMENT

A two metal layer test structure was fabricated using conventional 180nm node technologies and SiO_2 as the interlevel dielectric with SiN as the copper capping layer and etch stop. The concentration of organic additives in the copper-plating bath was varied to modulate the microstructure and physical properties of the copper. Both metal 1 and 2 used the same copper plating process and a post plate anneal condition of 150°C for one hour prior to CMP. Stress migration was characterized by measuring the resistance shift of single vias after a cyclic anneal from 150°C to 250°C. [8] The vias were 0.25μm in diameter with a 12 μm contact area of copper above and below the via. Three wafers were used for each experimental cell with 120 vias per wafer measured. The PVD barrier process used for this work had an aggressive Ar sputter preclean that is known to enhance stress migration failures. [4] The stress migration failure mode induced by this aggressive Ar sputter etch is a void in the Metal 1 layer under the via due to poor adhesion at the metal / dielectric interface. An alternative barrier process can reduce this effect by depositing a TaN barrier metal layer first and them performing the sputter clean such that resputtered copper is deposited on TaN and not a dielectric. This process improved the stress migration performance as shown in Figure 1. For the purpose of this study, we used the Ar sputter clean process with a large stress migration signal to magnify the effect of copper chemistry

RESULTS AND DISCUSSION

Via stress migration results for three different plating chemistries are shown in Figure 2. A degradation of stress migration performance is observed for chemistries 2 and 3 relative to chemistry 1. Analysis of the microstructure for copper deposited with each chemistry was done by FIB/SEM

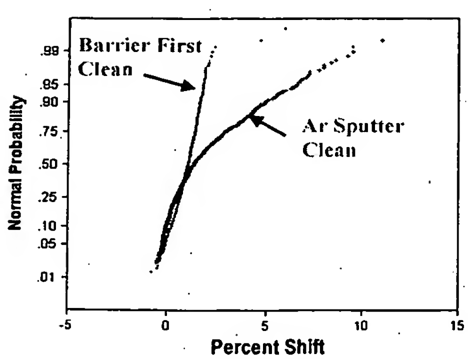

Figure 1: Resistance shift of an isolated Kelvin tester with two methods of via cleaning. The Ar sputter method leaves copper on the side walls of the via degrading adhesion.

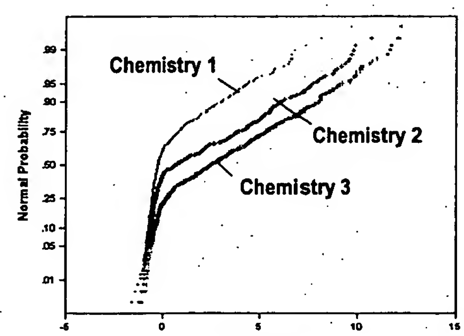

Figure 2: Resistance shift of an isolated Kelvin via tester for copper plated with three different chemistries.

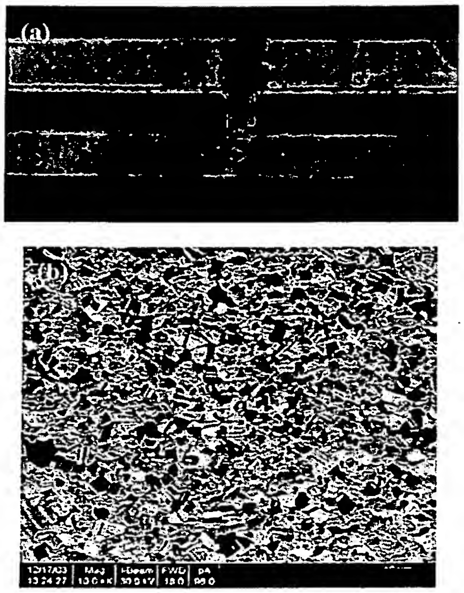

Figure 3: Grain structure in a Kelvin via (a) and bond pad (b) with copper deposited using chemistry 1 with improved stress migration.

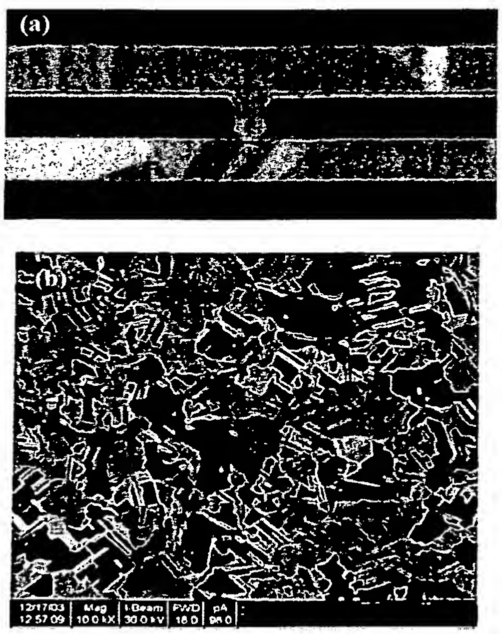

Figure 4: Grain structure in a Kelvin via (a) and in the bond-pads (b) for copper deposited using chemistry 3 with degraded stress migration.

and x-ray diffraction. Grain growth in the copper was complete after the post-plate anneal of 150°C and the 400°C dielectric deposition. No grain growth is expected during the thermal treatment used to induce stress migration. Both blanket films and the Kelvin stress migration testers showed

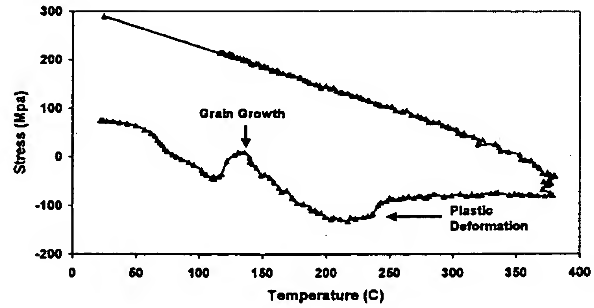

Figure 5: Stress temperature curves for the two chemistries. These curves were obtain after sever heat/cool cycles to eliminate work-hardening effects.

smaller grains for chemistry 1 (Figure 3) relative to chemistry 3 (Figure 4). The grain size was similar for chemistries 2 and 3. The observation of a smaller grain size but improved stress migration performance for chemistry 1 relative to chemistry 2 and 3 is contradictory to the model of void formation from the coalescence of vacancies from grain boundaries in the copper. [4] A high concentration of vacancies at the grain boundaries is required to account for the void volume that forms under a via. Smaller grains should increase the availability of vacancies and degrade via stress migration. However, we observe the opposite trend for copper deposited with chemistry 1 relative to chemistry 2 and 3.

The mechanical properties of the different copper films were examined by stress-temperature curves. [9, 10] Stress-temperature hysteresis is very useful in understanding the properties of electroplated copper. Figure 5 shows a typical stress vs. temperature curve for a blanket 0.8µm film on 150nm of copper seed and 25nm Ta(N) barrier. As deposited, the film had 50-100Mpa of tensile stress. Upon heating, the tensile stress is reduced due to the larger coefficient of thermal expansion for copper relative to Si. At a temperature of ~150°C, there is an increase in the copper tensile stress. This is the same temperature at which recovery/recrystallization of the copper occurs on the time scale of the ramp rate. Copper that has undergone recrystallization at room temperature before being heated does not show this inflection point in the stress. The tensile stress increases in the copper due to a reduction in vacancy and grain boundary concentration. It is important to note that the change in stress associated with recrystallization is ~ 40 MPa for this thickness of copper. The change in stress of the copper after the full temperature cycle is 200MPa. Therefore the dominate source of stress in copper films is the differential thermal contraction of the copper and not grain growth and recrystallization.

To make a quantitative comparison of the mechanical properties of copper, samples were prepared that best mimic the copper in encapsulated features. Copper films 0.8um thick were deposited from chemistries 1 and 3 on blanket wafers with a 25nm Ta(N) barrier and 100nm copper seed film. The copper was then annealed at 150°C for 1 hour for recrystallization and then polished back by CMP leaving a

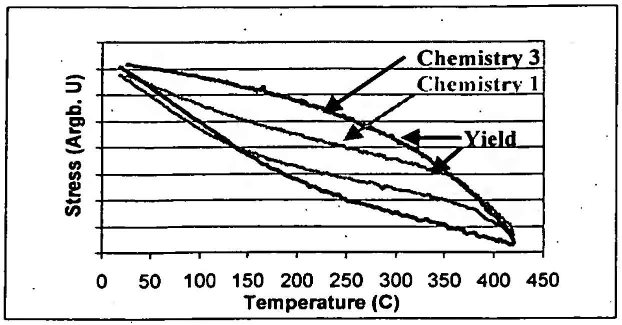

Figure 5: Stress temperature curves for the two chemistries. These curves were obtain after several heat/cool cycles to eliminate work-hardening effects.

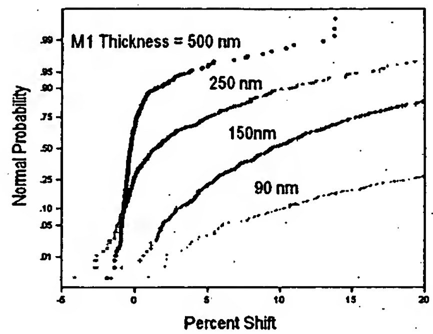

Figure 7: Via stress migration for a 250nm via with 4 different metal 1 thicknesses.

final Cu thickness of 0.7μm. The blanket wafers were then passivated with a 70nm SiN film and a 1μm of TEOS oxide at a deposition temperature of 400°C. The mechanical behavior of these passivated blanket copper films should be similar to the behavior of fully encapsulated wide copper lines such as those used in a stress migration testers. [3, 10] The absolute value of the stress in the copper is difficult to isolate from the stress in the dielectric above and below the copper, so values shown are in arbitrary units. Several heat/cool cycles were performed on the wafers to isolate the kinematic yield properties of the copper from dynamic yield properties such as work hardening. [11] The inelastic properties of copper films during a thermal cycle have been attributed to bulk deformation and interface controlled dislocation glide [9] or diffusional creep [10]. Figure 5 shows that the stress-temperature curves are very different for copper deposited with chemistry 1 relative to chemistry 3. The hysteresis curves are controlled by the yield stress of the copper. The yield stress can be inferred from the change in slope in the stress-temperature curve. [10] Differential thermal contraction of the copper relative to SiO_2 should have only one slope until the tensile stress of the copper exceeds the yield stress. At the yield point, the copper deformation becomes inelastic [9] and the slope of the stress-temperature curve changes to track the yield stress vs. temperature dependence. The hysteresis loop for the copper deposited with chemistry 1 is smaller due to a lower yield stress of the copper relative to chemistry 3. However, even with a difference in the yield points for the copper, the absolute stress level at ambient and at the stress migration temperatures of 200-250 °C are similar for the two copper films. Therefore, the stress level alone cannot account for the stress migration difference.

The above observations would indicate that there is a correlation between the yield properties of copper and stress migration. Copper with a lower yield stress (more ductile) has better stress migration performance than copper with a high yield stress (less ductile). An alternate method of modulating the stress of a copper film is to change the thickness. [12] For example, Figure 6 shows that the stress in a copper film after a thermal cycle to 350°C increases as the thickness is reduced. This phenomenon has been documented previously and is due to an increasing volume of copper that can deform as thickness is increased. [10, 12] Adhesion measurements with 4-pt bending show that copper films thicker than ~200nm have more volume available to plastically deform resulting in higher adhesion energies relative to thin copper films. [14]

Experiments were performed in which the metal 1 thickness was varied from 0.5μm to 0.1μm to modulate the stress of the

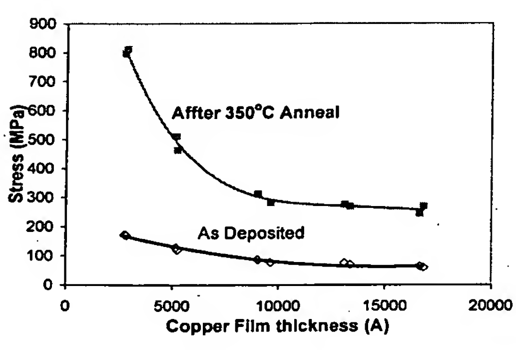

Figure 6: Stress for blanket films of copper deposited on 1000A of seed and annealed at 350°C for 1 hour..

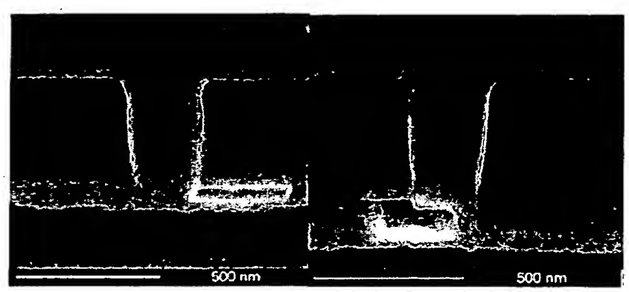

Figure 8: Voids under a 250nm via with (a) 100nm and (b) 250nm of metal 1 copper.

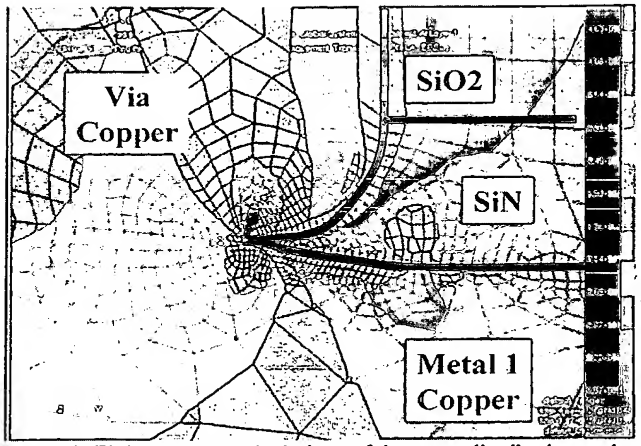

Figure 9: Finite element calculations of the stress distribution at the lower corner of a via. Blue regions are low stress, green regions are intermediate stress and yellow is high stress.

copper. All other dimensions of the via remained unchanged. The stress migration performance degraded substantially with reduced metal 1 thickness as shown in Figure 7. Failure analysis showed that the post anneal stress voids were larger in the 0.1μm film and formed along the SiN / copper interface as shown in Figure 8. The absolute via resistance did not change significantly with the reduced metal 1 thickness because the spreading resistance of the lower copper film is a small contribution to the total via resistance relative to the high resistivity barrier material at the bottom of the via. This result is opposite to the generally observed trend of improved via stress migration with reduced copper volume under a via due to fewer available vacancies. [4, 6] It would appear that stress gradients in the copper dominate the stress migration performance over the absolute number of vacancies.

Finite element analysis was performed of the stress levels in the copper within a confined via structure to understand how copper thickness and yield stress could effect via stress migration. All stress levels of the copper were set to zero initially and the structure was cooled by 200°C to simulate a thermal cycle from 400°C to 200°C. The largest thermally induced stress gradient in the copper were at the lower corner of the via at the SiN etch stop layer as shown in Figure 9. This is the same location where we observe nucleation of voids after stress migration tests as shown in Figure 8. [4] If we assume that these voids are due to the initiation of cracks or adhesion failure at the copper / SiN interface then the elastic and inelastic energy release rate can be calculated for copper with different yield stresses and thickness. [11] Two extreme examples were considered. A 0.1 μm thick layer of copper should have a yield stress of ~920 MPA and was found to have an *elastic* energy release rate of 10 mJ/m^2 but a *plastic* energy release rate of less than 0.1 mJ/m^2 for a 30nm crack initiation. In contrast, a 0.5μm thick layer of copper with a yield stress of 410MPa was found to have an *elastic* energy release rate of <0.1 mJ/m2 but a *plastic* energy release rate of 7 mJ/m^2 for a 30nm crack initiation. Therefore, the thick copper with a low yield stress had a higher *plastic* energy release rate and was therefore able to absorb the strain energy through plastic deformation without forming a crack.

Finite element calculations show that an increase in the thickness and / or a decrease in the yield stress of copper allows strain energy to be dissipated in the copper without forming a crack. If the yield stress of the copper is high, then the stress energy in the copper will go into the formation of a crack at the copper / SiN interface in the corner of a via. Once the crack is initiated, it can grow into a void through vacancy diffusion. The energy release rates calculated here are smaller than what is typically observed in 4-point bending adhesion measurements, but the length scales for the finite element calculations are 1E-9 m whereas 4-point bending test are done on a mm length scale. The absolute values of the calculated crack energies also depend strongly on the radius of curvature at the via bottom and the crack length used for the calculation. Therefore, a high degree of quantitative agreement between the finite element calculations and experimental 4-point bend values would not be expected.

Stress migration behavior that scales with the yield stress of copper is consistent with void formation that occurs through an elastic volume contraction of copper under high tensile stress. The size of a void (δV) that can form through contraction of a volume of copper V under a via would be given by

$$\delta V = \frac{V\sigma}{E} \qquad (1)$$

where σ is the local stress and E is the modulus. Contraction of a ~30μm^3 volume of copper under a via with a stress level of 300MPa would correspond to a void volume of ~0.1μm^3. This is similar to voids that are observed after a stress migration test. Therefore, much of the initial volume associated with a void could be due to simple thermal contraction and not vacancy diffusion. However, growth of the void would have to occur through vacancy diffusion with the characteristic temperature dependence that has been observed. [4] The vacancy concentration required to form a void from supersaturation of vacancies is larger than what is required to grow a pre-existing void. If there are no pre-existing voids and if the stress gradients in the copper are such that vacancy supersaturation does not occur, then there would be no stress migration induced failures because no voids could nucleate. If the local adhesion energy between the copper and barrier and the dielectric are lower at some location than the yield stress of the copper then a voids can nucleate due to poor adhesion with a volume given roughly by equation (1).

The stress migration results of Figure 1 demonstrate that there is a strong dependence of stress migration performance on the metal barrier process and pre-clean. [4, 6, 7] This is consistent with the critical dependence of metal/dielectric adhesion on stress migration performance in addition to copper grain structure. [4] The via pre-clean and PVD barrier deposition process would not have any impact on copper grain

structure yet there is a major impact on stress migration performance.

CONCLUSION

In conclusion, we have shown through a combination of chemistry variation, copper thickness variation and finite element calculation that the stress migration performance of copper dual damascene structures depends on the yield stress of the copper in the interconnect. Initiation of a void at the corner of a via is controlled by the high stress level of the copper after a thermal cycle. Once void initiation occurs, vacancy diffusion can cause the void to grow. Therefore, one of the most critical elements for the control for via stress migration in copper dual damascene interconnects is the elimination of nucleation sites for voids in a via through improved metal/dielectric adhesion.

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